REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on January 31, 2001, and the references cited therewith. In this Response, claim 61 is amended, no claims are canceled, and no claims have been added. Accordingly, claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are currently pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of Form 1449, listing all references that were submitted with the Information Disclosure Statement filed on September 30, 1999, marked as considered and initialed by the Examiner, be returned to the Applicant with the next official communication.

Double Patenting Rejection

In § 3 of the Office Action, claims 59-60 were provisionally rejected (under the judicially created doctrine of obviousness-type double patenting) as being unpatentable over claim 36 of co-pending U.S. Application Serial No. 08/984,563. In § 4 of the Office Action, claim 61 was provisionally rejected (under the judicially created doctrine of obviousness-type double patenting) as being unpatentable over claim 59 of co-pending U.S. Application Serial No. 08/984,561.

Co-pending U.S. Patent Application Serial Nos. 08/984,563 and 08/984,561 have not yet received any final indication of allowed claims. The Applicant requests that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending applications to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicant will submit a Terminal Disclaimer to obviate any remaining double patenting rejection upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

Claim Objections

In § 5 of the Office Action, claim 61 was objected to because of informalities. The Applicant has amended claim 61 to provide a proper antecedent basis for each element in the claim and to clarify when addresses are generated. As a result, after inspection by the Examiner, it is believed that claim 61 will now be in condition for allowance.

In § 6 of the Office Action, claims 1, 63 and 64 were objected to under 37 C.F.R. 1.75(b) as not substantially differing from each other. The Applicant respectfully submits that claims 1, 63, and 64 are clearly different from each other. In particular, claim 1 recites "mode circuitry configured to select between a burst mode and a pipelined mode", claim 63 recites "mode circuitry for receiving a burst/pipeline signal", and claim 64 recites "mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation". None of these elements is the same as either of the others; each has a clearly defined difference according to the recited elements.

For example, the mode circuitry of claim 1 is configured to select between a burst mode and a pipeline mode, and to pass the selection on to the "circuitry operable in either a burst mode or a pipelined mode". The mode circuitry of claim 63 actually receives the mode selection signal. The mode circuitry of claim 64 operates in either the burst mode or the pipeline mode, as determined by the burst/pipeline selection circuitry. Clearly, selecting a mode of operation is different from receiving a selection, which is in turn different from operating in a particular mode as the result of determination by another circuit. Thus, withdrawal of this objection is respectfully requested.

Claims 33, 59 and 60 were also objected to under 37 C.F.R. 1.75(b) as not substantially differing from each other. The Applicant respectfully submits that claims 33, 59, and 60 are also clearly different. In particular, claim 33 does not recite the step of "receiving a burst/pipeline signal", claim 59 does not recite the step of "selecting between outputting information from the storage device and inputting information to the storage device", while claim 60 recites both of these steps. Clearly, receiving a burst/pipeline signal and selecting whether a memory sends or receives data are different steps. Thus, withdrawal of this objection is also respectfully requested.

§102 Rejection of the Claims

In § 8 of the Office Action, claims 1-9, 33-35, 46, 48-50, 59-61 and 63-64 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning (U.S. Pat. No. 5,610,864). The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses the rejection by the Office.

The Office has failed to produce a *prima facie* case of anticipation. For example, the Applicant cannot find, and the Office has failed to show, where Manning discusses the ability to select between burst and pipelined *modes* of operation. The Office notes that Manning discusses a "pipelined architecture" at column 5, lines 43-50. Does Manning refer to individually addressing and accessing memory data in a pipelined fashion, as defined by the Applicant, or merely driving data outputs in a pipelined fashion while operating in a burst mode? According to Manning, the pipelined architecture is "where memory accesses are performed sequentially, but each access requires more than one cycle to complete." This definition doesn't appear to markedly differentiate pipelined addressing and access from burst operations. Thus, Manning merely discloses the possibility that a pipelined *architecture* (as opposed to a mode of operation) might be "applicable to the current invention" (without disclosing how such an application might occur). *See* Manning at Col. 5, lines 43-50. Moreover, while Manning does specifically discuss the option of "switching between burst EDO and standard EDO modes of operation", Manning never extends this idea to switching between the pipelined *mode of operation*, and a burst mode of operation. Thus, the assertion by the Office that "Manning discloses mode circuitry to select between fast page pipeline and burst, and circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuitry and configured to select between the two modes." is simply not supported using any of the teachings of Manning.

As the Applicant has previously explained, the EDO mode is a mode that extends the amount of time for which data is valid at the outputs of a DRAM (*See* the Applicant's specification at page 3, lines 19-21). The fast page mode is a mode that uses a row address strobe to latch a row address portion of a DRAM address (*See* the Applicant's specification at page 2, lines 12-13), while the pipelined mode is a mode that divides address information into

operational times such that the address information can be provided from an external source as a stream of data (*See* the Applicant's specification at page 8, lines 1-13). Moreover, the Applicant also specifically teaches *switching* between pipelined and burst modes of operation (*See* the Applicant's specification at page 26, line 24 - page 27, line 1).

The Applicant cannot find where Manning discusses that these mode are interchangeable, or combinable, such that the term "fast page pipeline" asserted by the Office can be defined. The Applicant still fails to understand the meaning of this phrase, and looks to the Office for a more detailed explanation. Thus, the Applicant cannot find, and the Office has failed to show, a single instance where Manning discusses memory activity using burst and pipelined *modes of operation*, or selecting between these *modes of operation*, as claimed by the Applicant in independent claims 1, 33, 46, 50, 59-61, and 63-64, and the claims which depend from them.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

CONCLUSION

The Applicant's representative has reviewed the other art made of record by the Office, but believes that the cited art is more pertinent to the instant application. Thus, the Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30 day of April, 2001.

Tina Pugh
Name

Signature